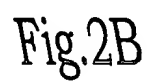
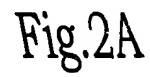


Fig.1



3/19

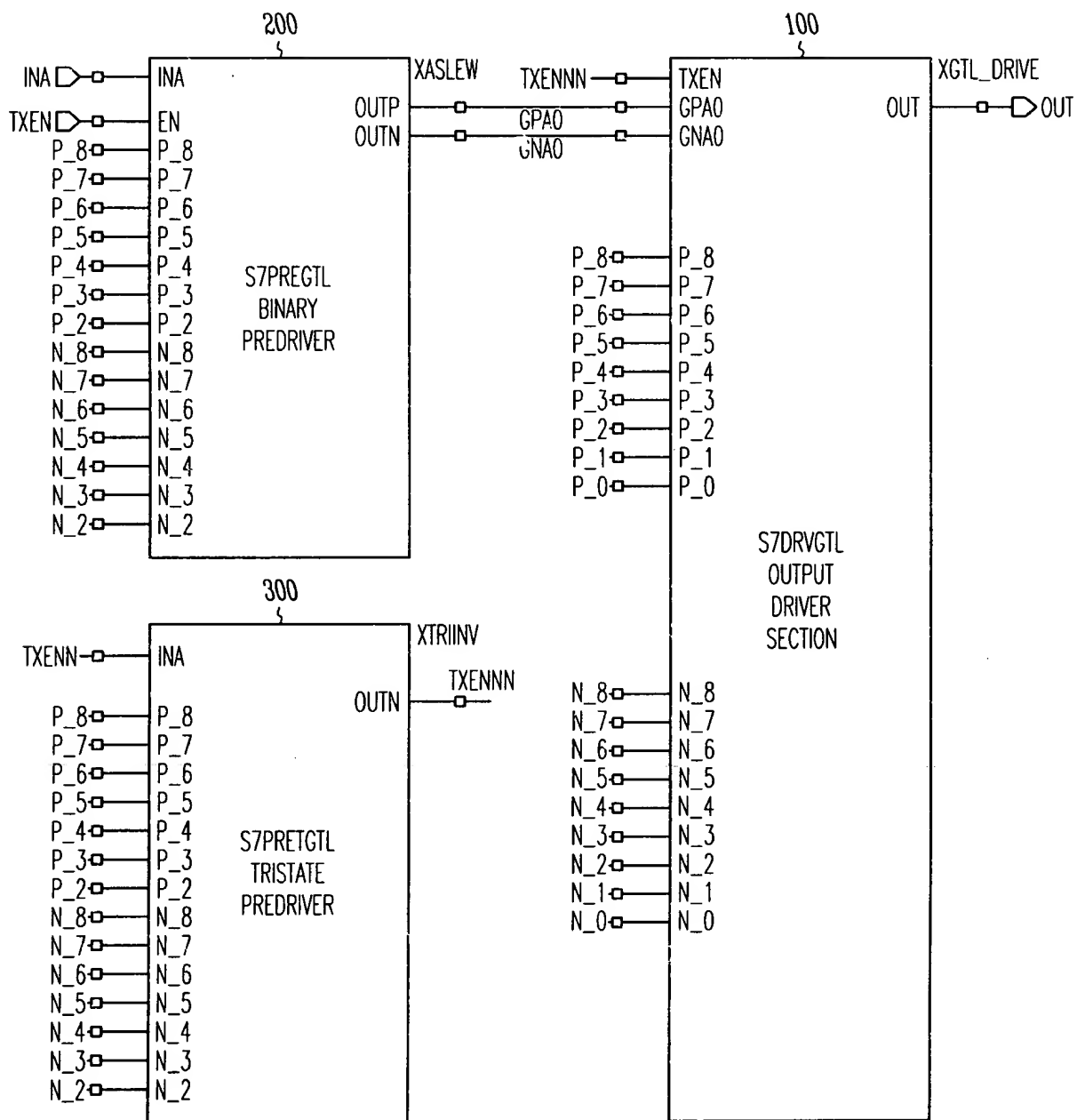
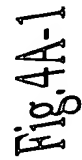
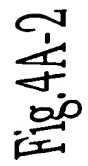


Fig.3





6/19

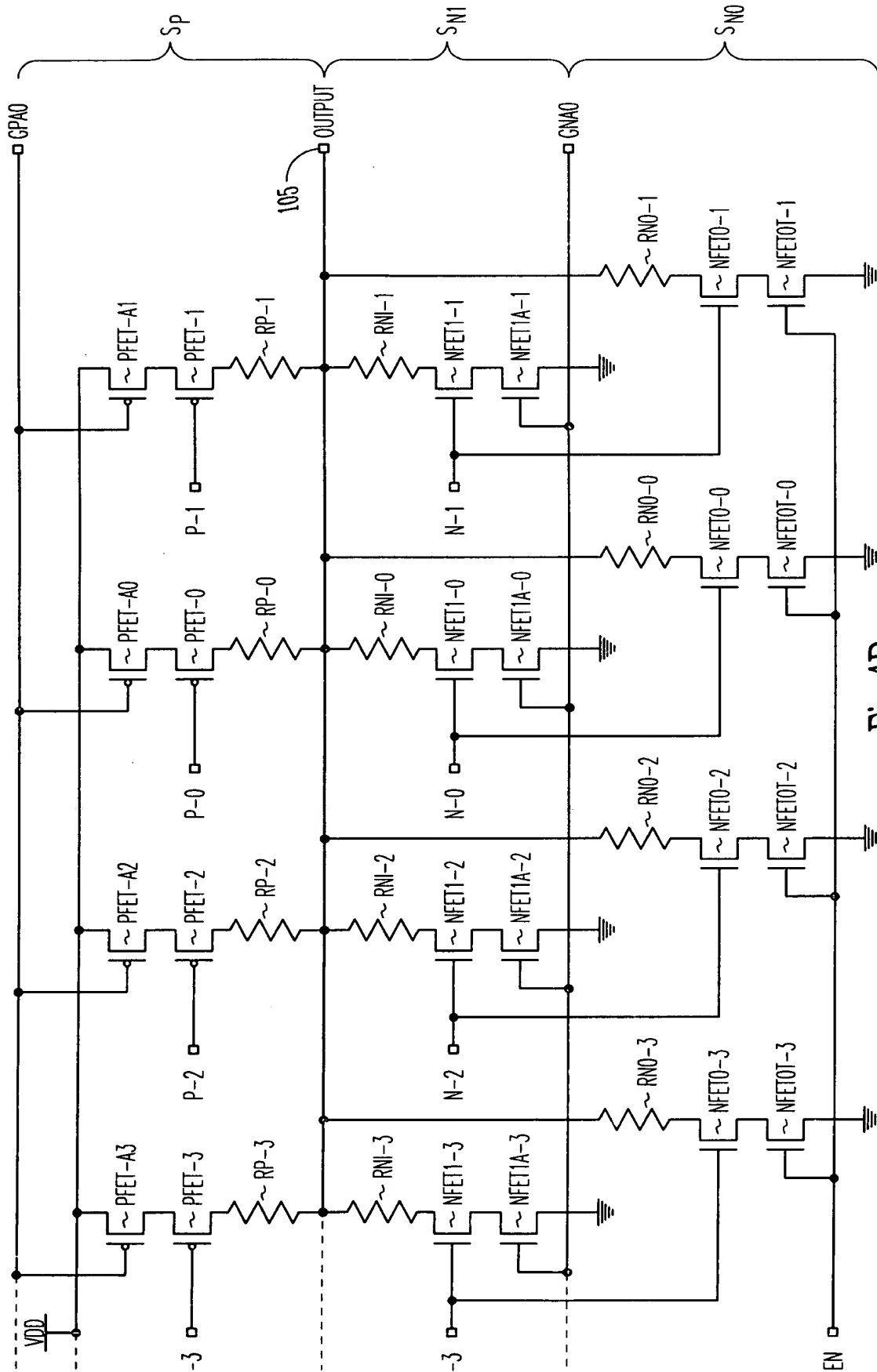
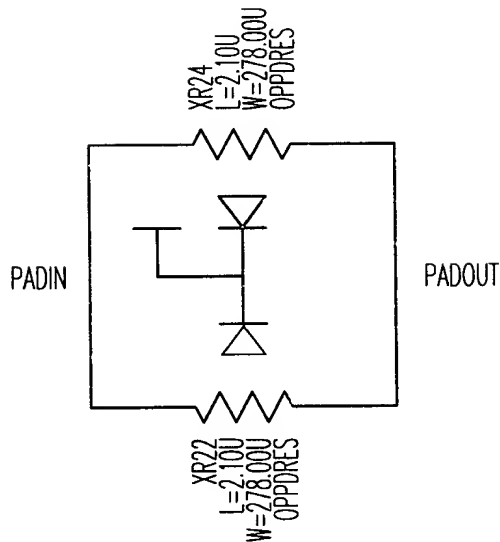


Fig.4B

TITLE: GTL + DRIVER
INVENTORS NAME: Rodney Ruesch
SERIAL NO.: 09/620,679

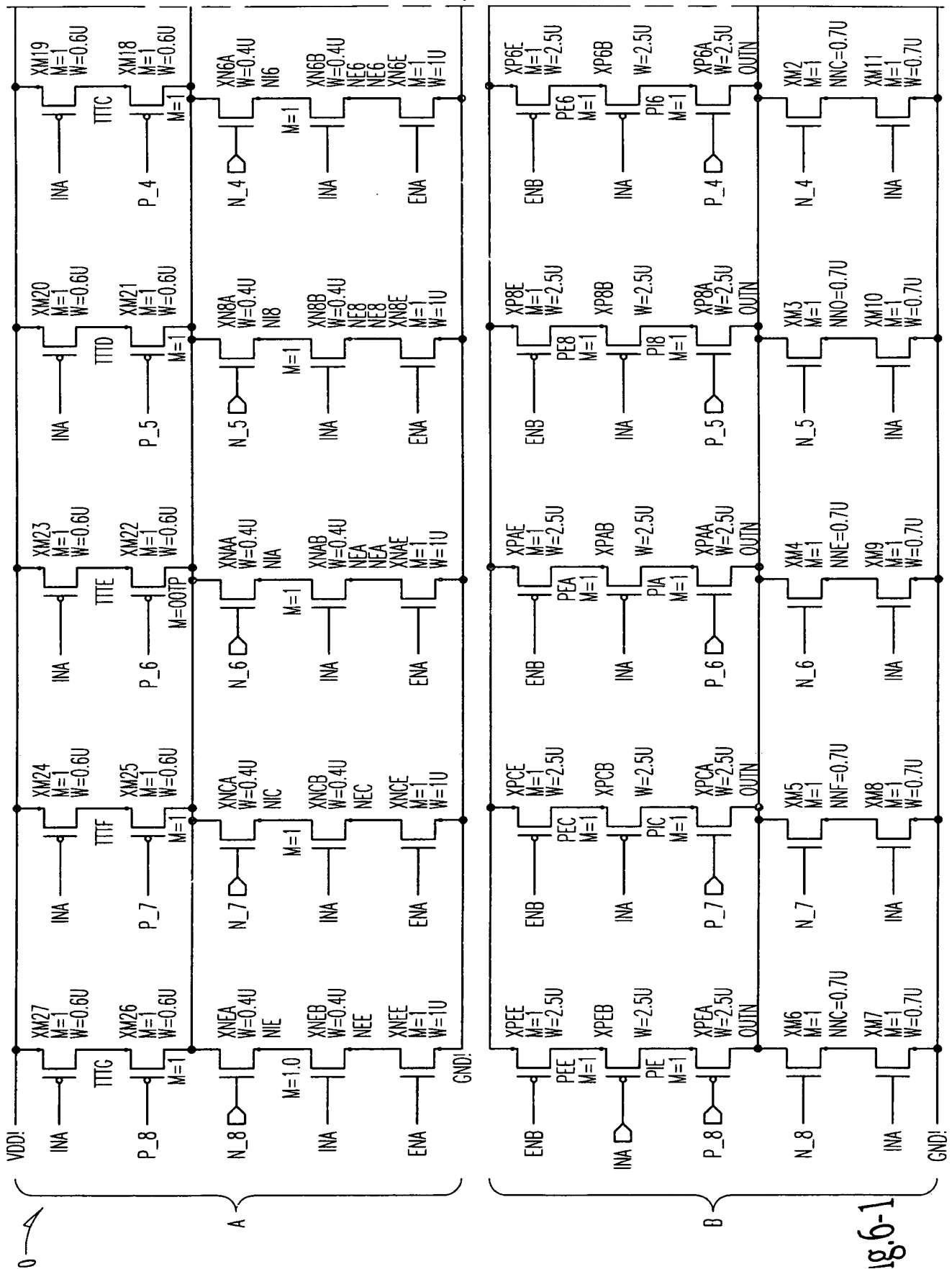
7/19



SELECTABLE OP RESISTORS TO BE USED WITH PADXFER METAL (LM) TOTAL RESISTANT MATCHING UP TO 3 OHMS

ONE RESISTOR L=2.1U AND W=93.0U = 3.0 OHMS
ONE RESISTOR L=2.1U AND W=111.0U = 2.5 OHMS
ONE RESISTOR L=2.1U AND W=139.0U = 2.0 OHMS
ONE RESISTOR L=2.1U AND W=185.0U = 1.5 OHMS
ONE RESISTOR L=2.1U AND W=278.0U = 1.0 OHMS
TWO RESISTORS L=2.1U AND W=278.0U IN PARALLEL = 0.5 OHMS SHOWN
ZERO RESISTORS TO BE USED FOR 0 OHMS

Fig.5



9/19

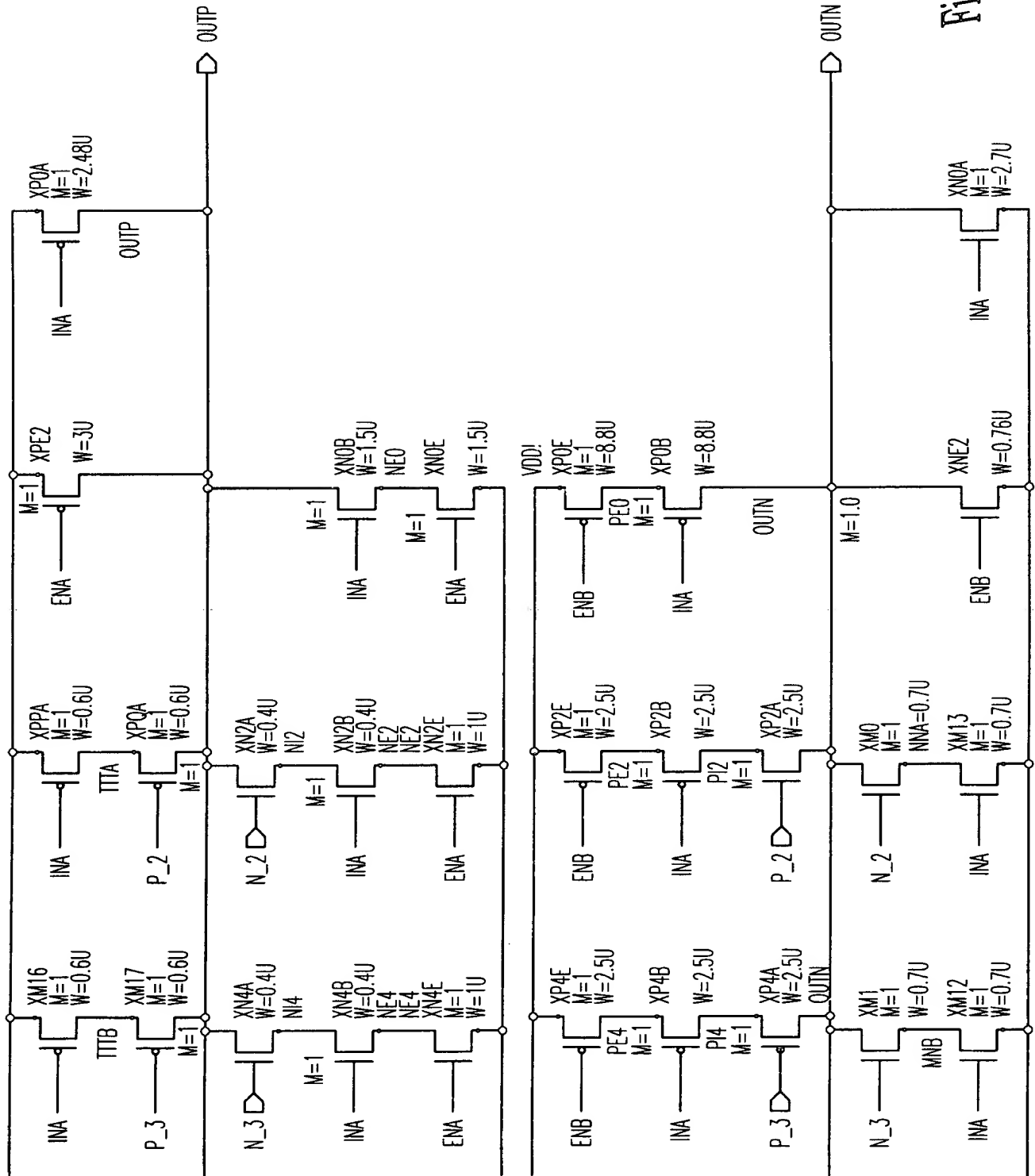


Fig. 6-2

10/19

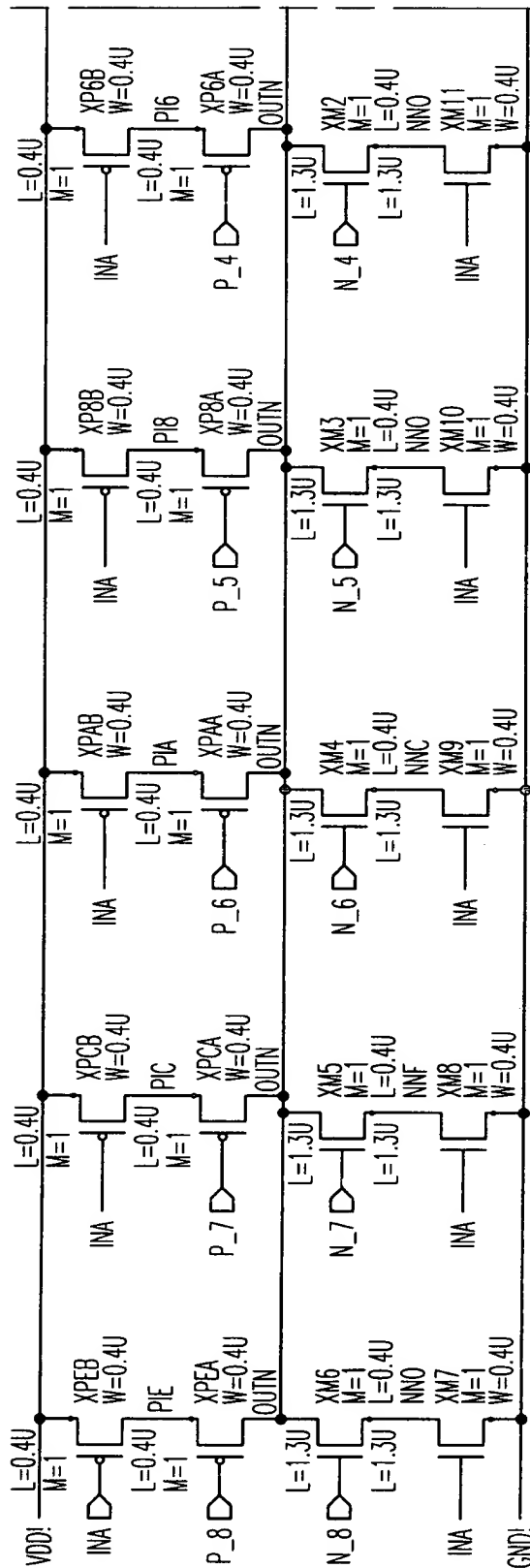


Fig.7-1

11/19

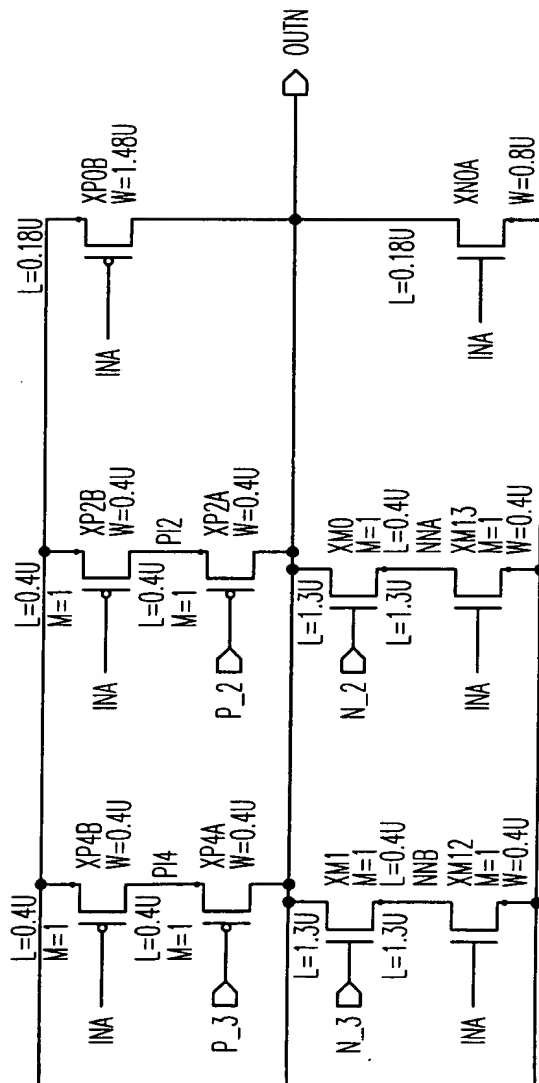


Fig. 7-2

12/19

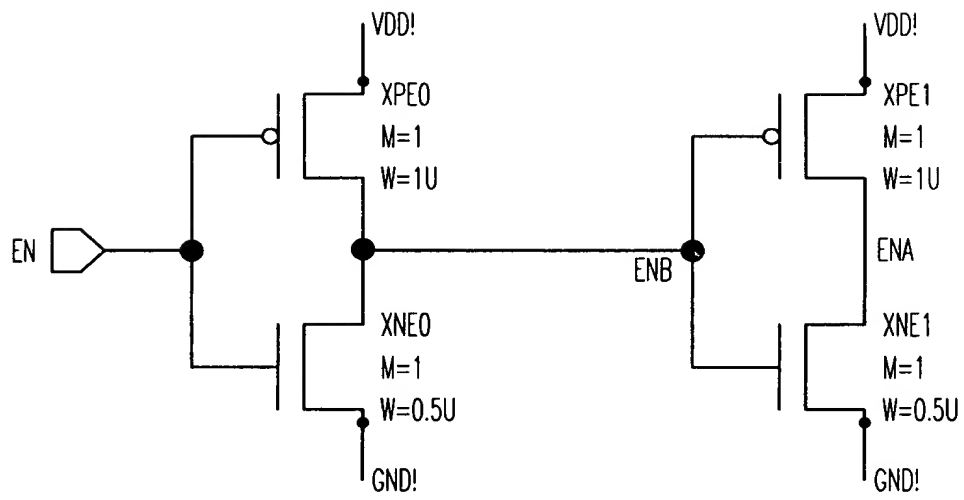
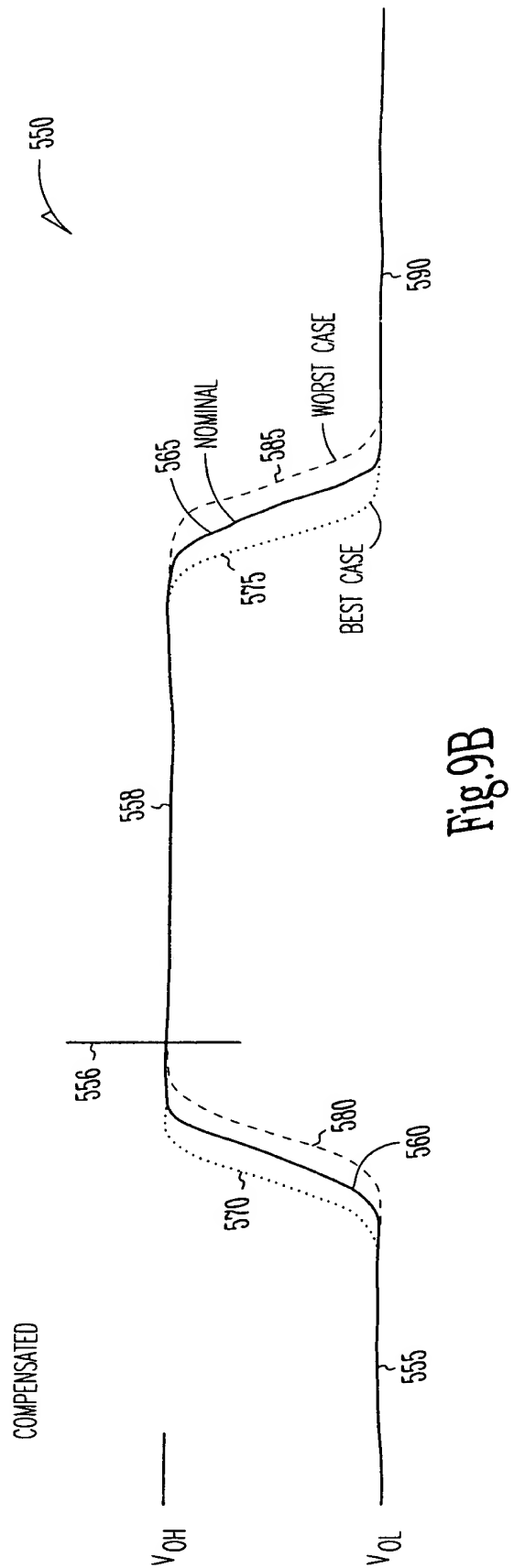
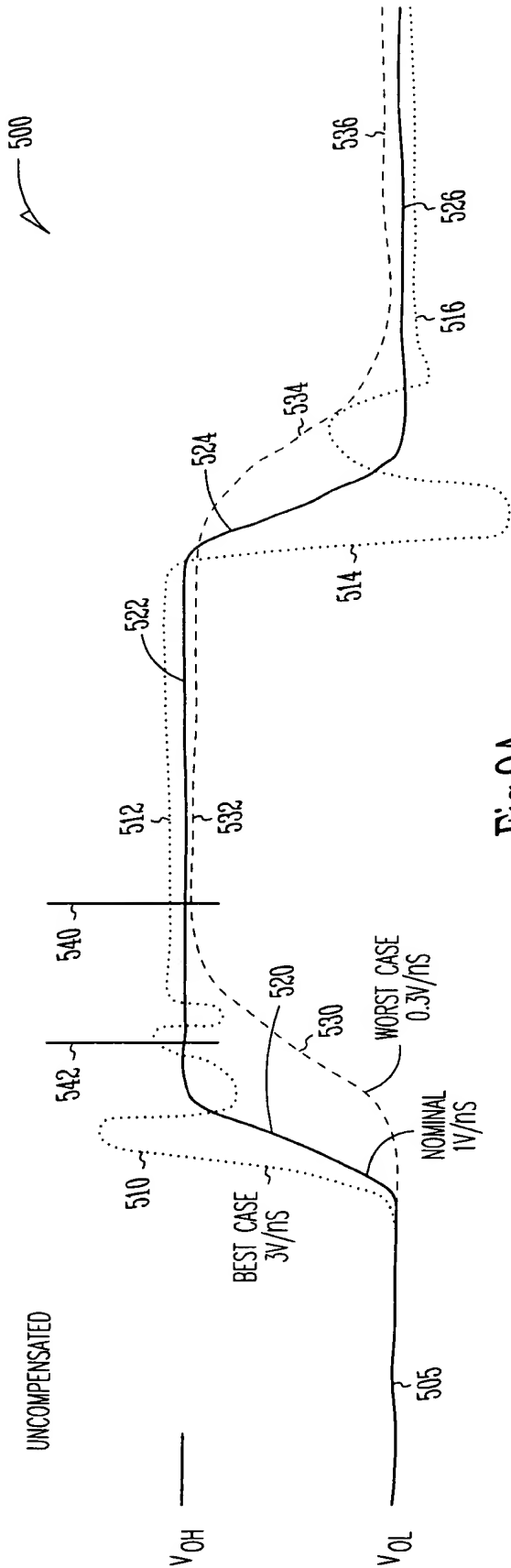


Fig.8



14/19

DESCRIPTION:

NON-INVERTING BI-DIRECTIONAL DRIVER/RECEIVER THAT INTERFACES 1.8V INTERNAL FUNCTIONS WITH 1.1V ENHANCED GTL+ OFF-CHIP BI-DIRECTIONAL DATA BUS. THE DRIVER OPERATES WITH A 1.8V SUPPLY. THE DRIVER HAS OFF-CHIP TERMINATION OF 45 OHM TO 1.1V (V_{TT}) AT EACH END OF THE BUS (DOUBLE TERMINATION). THE RECEIVER HAS EXTERNAL REFERENCE V_{ref} ($V_{TT} * 2/3$).

A0	DRIVER DATA0 INPUT
A1	DRIVER DATA1 INPUT
AN0	DRIVER DATA0 INPUT
AN1	DRIVER DATA1 INPUT
SA	DRIVER DATA SELECT INPUT
DI	DRIVER INHIBIT INPUT (DI IN)
TS	IN-PHASE DRIVER THREE-STATE CONTROL
TSN	OUT-PHASE DRIVER THREE-STATE CONTROL
PVTP[8:0]	PMOS EDGE RATE CONTROL BUS INPUT
PVTN[8:0]	NMOS IMPEDANCE CONTROL BUS INPUT
RE	REFERENCE ENABLE
RI	RECEIVER INHIBIT INPUT (RI IN)
VREF	($V_{TT} * 2/3$) INPUT SIGNAL
PAD	IN-PHASE DRIVER OUTPUT/RECEIVER INPUT
PADN	OUT-PHASE DRIVER OUTPUT/RECEIVER INPUT
ZDI	DRIVER INHIBIT OUTPUT (DI OUT)
ZRI	RECEIVER INHIBIT OUTPUT (RI OUT)
Z	IN-PHASE RECEIVER OUTPUT
ZN	OUT-PHASE RECEIVER OUTPUT
ZA	DATA0 TEST OUTPUT (A0 OR A1 OUT)
ZAN	DATANO TEST OUTPUT (AN0 OR AN1 OUT)
ZBSR	PAD TEST OUTPUT (PAD OUT)
ZNBSR	PADN TEST OUTPUT (PADN OUT)
LT	LEAKAGE TEST INPUT

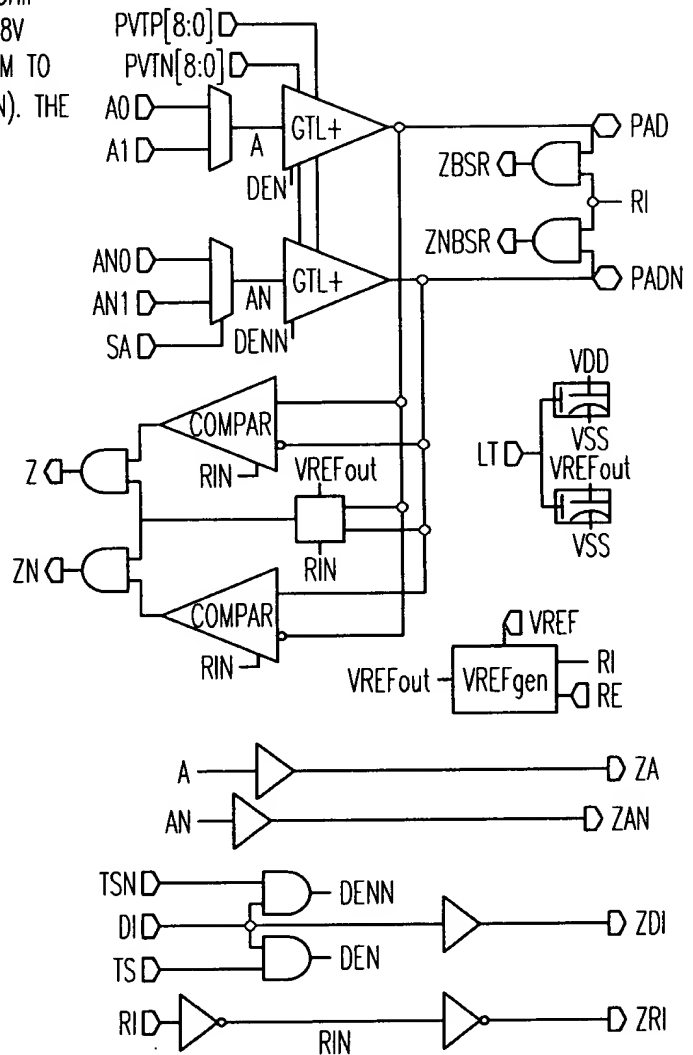


Fig.10

15/19

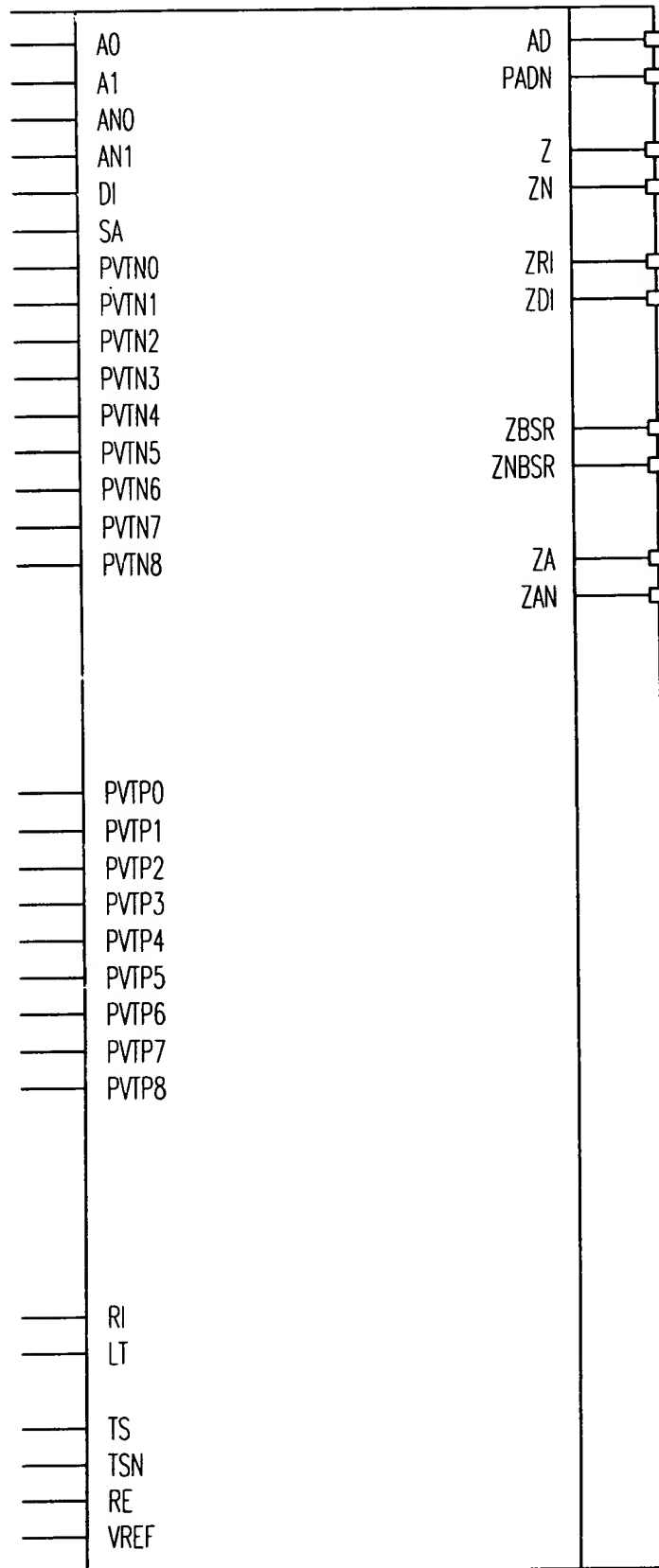


Fig.11

16/19

DRIVER TRUTH TABLE

INPUTS					OUTPUTS			
A0	A1	SA	IS	DI	PVTP	PVTN	PAD	COMMENTS
-	-	-	0	-	-	-	HI-Z ¹	HIGH IMPEDANCE MODE
-	-	-	-	0	-	-	HI-Z ¹	HIGH IMPEDANCE MODE
-	-	-	-	-	0 ²	0 ²	HI-Z ¹	PVT TEST MODE
0	-	0	-	-	-	0 ²	HI-Z ¹	PVT TEST MODE
1	-	0	-	-	0 ²	-	HI-Z ¹	PVT TEST MODE
0	-	0	1	1	-	>0	0 ³	PVT TEST MODE ³
1	-	0	1	1	>0	-	1 ³	PVT TEST MODE ³
0	-	0	1	1	>0	>0	0 ³	FUNCTIONAL, A0 DATA MODE
0	-	0	1	1	1	1	0 ³	FUNCTIONAL, 10 OHMS @ BC
0	-	0	1	1	4	4	0 ³	FUNCTIONAL, 10 OHMS @ NOM
0	-	0	1	1	8	8	0 ³	FUNCTIONAL, 10 OHMS @ WC
1	-	0	1	1	>0	>0	1 ³	FUNCTIONAL, A0 DATA MODE
-	-	1	1	1	>0	>0	A1	FUNCTIONAL, A1 DATA MODE

1. PAD IS AT "V_{TT}" WHEN CONNECTED TO OFF-CHIP TERMINATOR.

2. WHEN PVT=0 ALL PVT BITS GO TO V_{SS} AND ARE OFF.

3. PAD LOGICAL "1"=V_{HT}=1.1V, LOGICAL "0"=0.4V OR LESS.

NOTES: A. V_{dd}=1.8(+/-0.1)V, V_{HT}=1.1(+/-0.02)V

B. DURING MODULE EXTERNAL I/O TEST AND SYSTEM MODE, DRIVER OUTPUT PULLUP IS MADE

BY THE EXTERNAL 22.5 OHM RESISTOR TO V_{HT}.

C. NDR WILL BE BASED ON DRIVER TERMINATED OFF-CHIP.

D. A0, A1, AN0, AND AN1 ARE INDEPENDENT FROM EACH OTHER.

E. ENTRIES IN COLUMNS PVTP, PVTN REPRESENT NUMBER OF LINES HELD AT LOGIC "1"

STATE. FOR TESTING, THE IMPEDANCE CONTROLLER FORCES PVTP AND PVTN TO 4

(i.e. PVTP[8:0]=PVTN[8:0]=[000011110]) FOR ALL SUPPLY VOLTAGE LEVELS.

Fig.12

17/19

DRIVER TRUTH TABLE

INPUTS					OUTPUT		
AN0	AN1	SA	TSN	DI	PVTP	PVTN	COMMENTS
-	-	-	0	-	-	-	HI-Z ¹ HIGH IMPEDANCE MODE
-	-	-	-	0	-	-	HI-Z ¹ HIGH IMPEDANCE MODE
-	-	-	-	-	0 ²	0 ²	HI-Z ¹ PVT TEST MODE
0	-	0	-	-	-	0 ²	HI-Z ¹ PVT TEST MODE
1	-	0	-	-	0 ²	-	HI-Z ¹ PVT TEST MODE
0	-	0	1	1	-	>0	0 ³ PVT TEST MODE ³
1	-	0	1	1	>0	-	1 ³ PVT TEST MODE ³
0	-	0	1	1	>0	>0	0 ³ FUNCTIONAL, A0 DATA MODE
0	-	0	1	1	1	1	0 ³ FUNCTIONAL, 10 OHMS @ BC
0	-	0	1	1	4	4	0 ³ FUNCTIONAL, 10 OHMS @ NOM
0	-	0	1	1	8	8	0 ³ FUNCTIONAL, 10 OHMS @ WC
1	-	0	1	1	>0	>0	1 ³ FUNCTIONAL, A0 DATA MODE
-	-	1	1	1	>0	>0	A1 FUNCTIONAL, A1 DATA MODE

1. PAD IS AT "V_{TT}" WHEN CONNECTED TO OFF-CHIP TERMINATOR.
 2. WHEN PVT=0 ALL PVT BITS GO TO V_{SS} AND ARE OFF.
 3. PAD LOGICAL "1" = V_{TT} = 1.1V, LOGICAL "0" = 0.4V OR LESS.
- NOTES: A. V_{dd} = 1.8(+/-0.1)V, V_{TT} = 1.1(+/-0.02)V

- B. DURING MODULE EXTERNAL I/O TEST AND SYSTEM MODE, DRIVER OUTPUT PULLUP IS MADE BY THE EXTERNAL 22.5 OHM RESISTOR TO V_{TT}.
- C. NDR WILL BE BASED ON DRIVER TERMINATED OFF-CHIP.
- D. A0, A1, AN0, AND AN1 ARE INDEPENDENT FROM EACH OTHER.
- E. ENTRIES IN COLUMNS PVTP, PVTN REPRESENT NUMBER OF LINES HELD AT LOGIC "1" STATE. FOR TESTING, THE IMPEDANCE CONTROLLER FORCES PVTP AND PVTN TO 4 (i.e. PVTP[8:0] = PVTN[8:0] = [000011110]) FOR ALL SUPPLY VOLTAGE LEVELS.

Fig.13

18/19

RIVER PROPAGATION DELAYS (NO LOAD ON OUTPUTS)			DELAY (ns)=INTERCEPT+SLOPE (D _{std}) ¹	
PATH (INPUT TO OUTPUT)	PERFORMANCE LEVEL	PARAMETER	$V_{dd}=1.7V$ $V_{th}=1.08V$ $T_j=100^{\circ}C$ PROCESS=SLOW	$V_{dd}=1.8V$ $V_{th}=1.13V$ $T_j=60^{\circ}C$ PROCESS=NOM.
AO-PAD	A	t _{PLH}	1.2ns	1.0ns
		t _{PHL}	1.2ns	1.0ns
ANO-PADN	A	t _{PLH}	1.2ns	1.0ns
		t _{PHL}	1.2ns	1.0ns
				$V_{dd}=1.9V$ $V_{th}=1.12V$ $T_j=25^{\circ}C$ PROCESS=FAST

1. D_{std} IS THE NUMBER OF STANDARD LOADS.
2. VOLTAGE AT THE PACKAGE PIN.
3. DESIGN IS OPTIMIZED FOR V_{th}=1.1V, CAN BE USED FOR V_{th}=1.0V TO 1.2V.

Fig.14

19/19

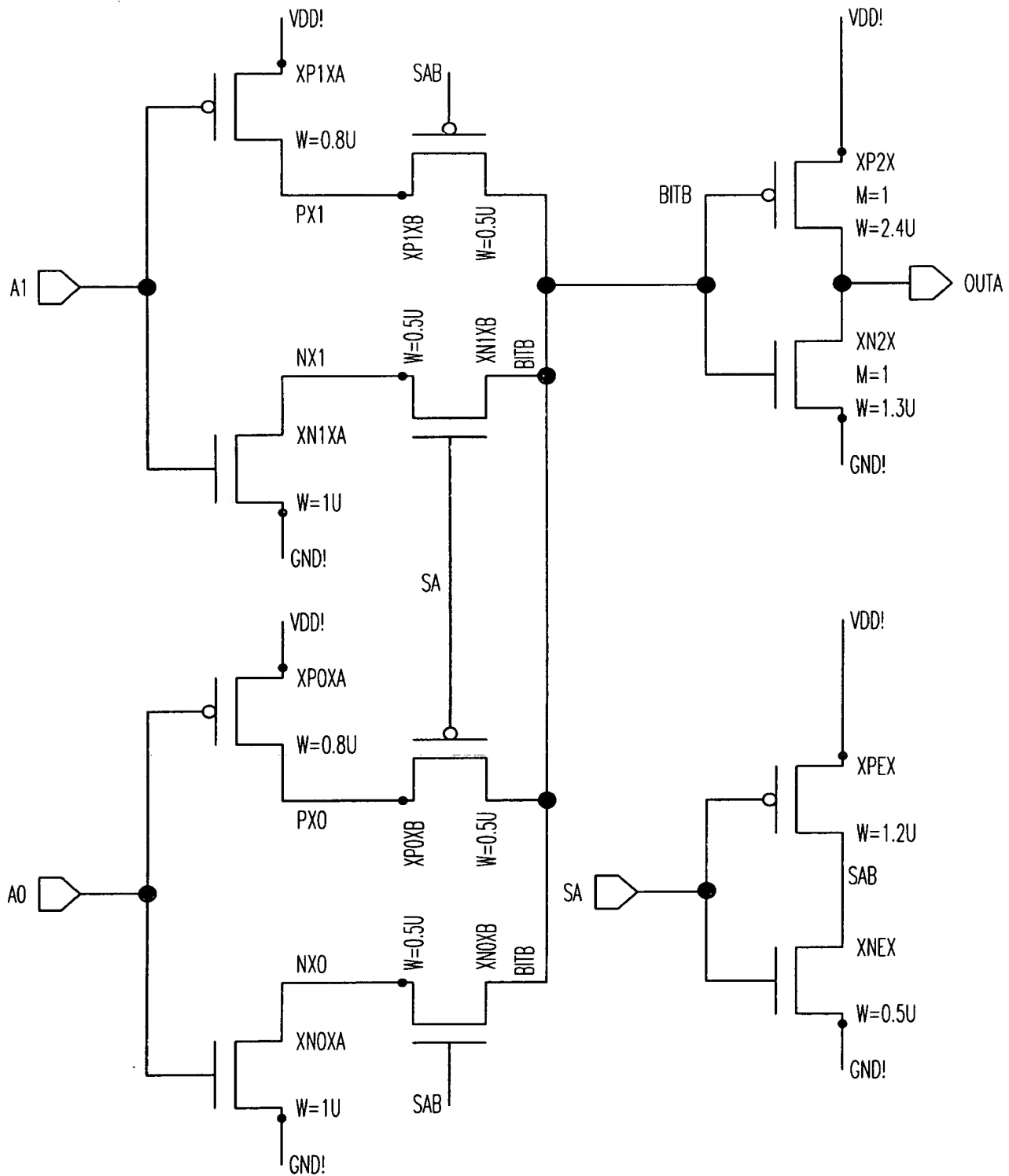


Fig.15